AMENDMENTS TO THE CLAIMS

Please cancel Claims 41-44, 52, 54-59, 67, 71, 73-75, and 77-92 without prejudice, as indicated below.

1.-92. (Cancelled)

93. (Previously Presented) A method for defining a system specification for a digital system, said method comprising the steps of:

partitioning said system into a plurality of processes, each of the processes having a defined behavior and each of the processes having at least one control thread;

defining separately from said processes a single data independent data communication protocol for communication within said digital system and between said processes;

configuring data communication interfaces in the form of communication input ports and communication output ports for each of the processes, the communication ports forming memory free communication channels, said step of configuring data communication interfaces involving defining communication interfaces with input ports of a first process and output ports to provide unidirectional, point-to-point connections between input ports of a first process and output ports of a second process, said input ports and said output ports being part of the associated processes, said processes implemented in C, Silage or VHDL language; and

combining the results of the steps of partitioning, defining and configuring to define specifications for said plurality of processes to form said system specification.

94. (Previously Presented) A method of implementing a digital system comprising the steps of:

partitioning said system into a plurality of processes, each process having a defined behavior and with at least one control thread;

defining separately from said processes, a single data independent data communication protocol for communication within said digital system and between said processes;

organizing said data communication protocol with input and output ports for said processes, said ports using memory free communication channels; and

designing a plurality of processors to implement said process, said step of designing processors comprising the step of specifying a processor having specification which conforms to the processes implemented, said processor comprising a programmable digital signal processor, wherein said plurality of specifications are selected from a group consisting of Silage descriptions, C descriptions, VHDL process descriptions.

95. (Previously Presented) A method of implementing a digital system comprising the steps of:

partitioning said system into a plurality of processes, each process having a defined behavior and with at least one control thread;

defining separately from said processes, a single data independent data communication protocol for communication within said digital system and between said processes;

organizing said data communication protocol with input and output ports for said processes, said ports using memory free communication channels implemented as interrupt driven I/O; and

designing a plurality of processors to implement said process, said step of designing processors comprising the step of specifying a processor having specification which conforms to the processes implemented.

96. (Previously Presented) A method of implementing a digital system comprising the steps of:

partitioning said system into a plurality of processes, each process having a defined behavior and with at least one control thread;

defining separately from said processes, a single data independent data communication protocol for communication within said digital system and between said processes;

organizing said data communication protocol with input and output ports for said processes, said ports using memory free communication channels, said communication channels implemented in integrated circuit form for communications between a first processor and a second processor across said channel, said first and second processors selected from one or more of a plurality of processor types, wherein said plurality of

processor types consists of Cathedral-III processors, ARM processors and VHDL generated processors; and

designing a plurality of processors to implement said process, said step of designing processors comprising the step of specifying a processor having specification which conforms to the processes implemented, said processor comprising a programmable, general purpose processor.

97. (Previously Presented) A method of implementing a digital system comprising the steps of:

partitioning said system into a plurality of processes, each process having a defined behavior and with at least one control thread, said step of partitioning involving defining a library of auxiliary processes to simulate the digital system, the library of processes selected from a plurality of processes consisting of one or more of an interactive I/O process, a file I/O process, a graphical output process, a channel duplicator process, a channel merging process, a FF process, a slider process, a button process, a first-in, first-out buffer process, an ARM processor, a digital to analog conversion process and an analog to digital conversion process;

defining separately from said processes, a single data independent data communication protocol for communication within said digital system and between said processes;

organizing said data communication protocol with input and output ports for said processes, said ports using memory free communication channels; and

designing a plurality of processors to implement said process, said step of designing processors comprising the step of specifying a processor having specification which conforms to the processes implemented, wherein said processor comprises a programmable digital signal processor.